UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/035,567	10/22/2001	Rebecca Yuan	WIDC-021/00US	3737

7590 05/03/2005

Kevin J. Zimmer
Cooley Godward LLP
Five Palo Alto Square
3000 El Camino Real
Palo Alto, CA 94306-2155

EXAMINER	
TRAN, KHANH C	

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 05/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/035,567	YUAN, REBECCA	
	Examiner	Art Unit	
	Khanh Tran	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5-28* is/are rejected.

7)☒ Claim(s) *4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03/20/2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07/08/2002*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 3 is objected to because of the following informalities: in line 1, claim does not define *the first sample sum*; see also page 8-9, paragraph [0021] of the original disclosure. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3, 5-6, 11 and 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Giallorenzi et al. U.S. Patent 5,867,525 in view of Chalmers U.S. Patent 6,141,372.

Regarding claim 1, in column 6, lines 20-51, figure 2 of Giallorenzi et al. invention discloses a portion of a radio base unit (RBU) 26 which handles one user k. The timing offset estimator for each user operates on a stream of samples of the aggregate CDMA received signal.

The aggregate CDMA waveform from various users is received at antenna 28 and is downconverted by radio frequency (RF) front end 30 to near baseband. RF front end 32 produces the downconverted aggregate waveform as both in-

phase (I) and quadrature phase (Q) outputs. The foregoing teachings correspond to the claimed step of "*receiving a data signal*".

In column 6 line 65 through column 7 line 60, in receiver 36, the in-phase (I) and the quadrature phase (Q) samples from bus 38 are rotated with a digital phase shifter (DPS) 40 and then despread using the PN code for user k in the RBU 36 for user k. The output of DPS 40 is then provided to three different despreaders: on time despreader 42, early despreader 44, and late despreader 46. Early despreader 44 includes multiplier 58 and an accumulator 59. In the abstract, Giallorenzi et al. teaches that in order to reduce noise effects, the offset estimate is averaged over a predetermined time duration and such averaging can be performed on the outputs of the despreaders. In light of the foregoing teachings, accumulator 59 accumulates first samples and performs averaging on the accumulated samples. Hence, the foregoing step corresponds to the claimed steps of "*accumulating a first sample sum value ...*" and "*computing a first averaged sample sum ...*".

Similarly, on time despreader 42 includes multiplier 56 and an accumulator 55, which accumulates second samples and performs averaging on the accumulated samples. Hence, the foregoing step corresponds to the claimed steps of "*accumulating a second sample sum value ...*" and "*computing a second averaged sample sum ...*".

Late despreader 46 includes multiplier 60 and an accumulator 61, which accumulates third samples and performs averaging on the accumulated samples.

Hence, the foregoing step corresponds to the claimed steps of "*accumulating a third sample sum value ...*" and "*computing a third averaged sample sum ...*".

Giallorenzi et al. further teaches in the Abstract that the outputs of the three despreaders are digitally combined or compared to produce the timing offset estimate for that user. The foregoing disclosure corresponds to the claimed step of "*identifying the maximum ...*" and "*generating an output symbol corresponding to the identified maximum*".

Giallorenzi et al., however, does not teach the received samples being DC compensated samples of the received data signal as claimed the application claim. Chalmers invention is directed to system for digitally downconverting and despreading a multi-channel analog direct sequence spread spectrum signal. Shown in figure 4, the system employs punctual complex signal (in-phase and quadrature components), complex early and late signals for estimating timing error signal. In column 9, lines 15-25, Chalmers teaches that any DC offset in the signal prior to A/D downconversion would be shifted into the stop band of the polyphase filter by the digital downconverters 510 512 and effectively removed. As also discussed in column 2 lines 19-25, because DC offsets are a concern and should be removed prior to demodulation, one of ordinary skill in the art at the time of the invention would have been motivated that Giallorenzi et al. receiver can be modified to remove the DC offsets before the demodulation step as taught in Chalmers invention. DC offset at baseband is often caused by a frequency offset at the receiver relative to the transmitter. As result of that, DC

offset estimation is required to eliminate a residual DC signal resulting from the process of down-converting the received signal to baseband.

Regarding claim 2, in column 13, lines 1-50, see also figure 3, Giallorenzi et al. expressly teaches that if it is necessary to know whether the offset is early or late, then the sign of the difference E-L (early – late) should be reserved. In view of that, the timing offset estimate is of a value when the difference E-L is positive and is otherwise of a second value as claimed in the application claim.

Regarding claim 3, as recited in claim 1, early accumulator 59 accumulates first samples and performs averaging on the accumulated samples. Hence, the first sample sum value is inherently defined as claimed in the application claim.

Similarly, on time despreader 42 includes multiplier 56 and an accumulator 55, which accumulates second samples and performs averaging on the accumulated samples. Hence, the second sample sum value is inherently defined as claimed in the application claim.

Late despreader 46 includes multiplier 60 and an accumulator 61, which accumulates third samples and performs averaging on the accumulated samples. Hence, the third sample sum value is inherently defined as claimed in the application claim.

Regarding claim 5, as recited in claim 1, as recited in claim 2, when the difference E-L is negative, the timing offset estimate is late (L), corresponding to the claimed third sample sum. Hence, the symbol timing is adjusted toward late sample, see figure 4.

Regarding claim 6, because the late symbol is n+1 and the timing offset estimate is late, the next symbol timing is set to n+1 as claimed in the application claim.

Regarding claim 11, in column 12 lines 40-67, Giallorenzi et al. teaches that if the user sending that signal is off synchronization by a sample, it might be that the first sample made at receiver 36 would actually be the 256th half chip of the previous bit and the second sample would instead be the first half chip of the new bit, while the third sample would be the second half chip of the new bit, and so forth. Accordingly, it is necessary to be able to identify whether an incoming signal is properly synchronized and to accomplish proper synchronization of one or more subscriber units. To address this problem, receiver 36 includes not only on-time despreader 42, but also early despreader 44 and late despreader 46. FIG. 3 shows a triangle autocorrelation function. In FIG. 2, the early sample value E and the late sample value L are shown as being at different heights because the autocorrelation function for the signals that are being received is triangular within about plus or minus one chip of the correct alignment. In view of the foregoing disclosure, the set of early samples and the second set of on-time samples are offset by one sample.

Regarding claim 19, claim 19 is rejected on the same ground as for claim 2 because of similar scope.

Regarding claim 20, claim 20 is rejected on the same ground as for claim 5 because of similar scope.

Regarding claim 21, claim 21 is rejected on the same ground as for claim 6 because of similar scope.

3. Claims 7-9 and 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Giallorenzi et al. U.S. Patent 5,867,525 and Chalmers U.S. Patent 6,141,372. as applied to claim 1 above, and further in view of Dutkiewicz et al. U.S. Patent 5,629,960.

Regarding claim 7, Giallorenzi et al. and Chalmers do not teach the step of computing a DC offset estimate as claimed. Dutkiewicz et al. invention is directed to a method for reducing the effects of transients on the DC offset tracking stage and the symbol timing recovery stage. In column 3 line 25 via column 4 line 25, figure 3 discloses a system including an analog-to-digital (A/D) converter 22, a DC offset removal 22, a DC tracking stage 23, and a symbol timing recover stage 25. The DC tracking stage tracks the mean DC offset and provides a DC offset voltage 32. Giallorenzi et al., Chalmers and Dutkiewicz et al. teachings are in the same field of endeavor. As recited in claim 1, DC offset at baseband is often caused by a frequency

offset at the receiver relative to the transmitter. As result of that, DC offset estimation is required to eliminate a residual DC signal resulting from the process of down-converting the received signal to baseband. In view of that, it would have been obvious for one of ordinary skill in the art at the time of the invention that Giallorenzi et al. teachings can be modified to implement DC offset removal and DC tracking stage as taught in Dutkiewicz et al. invention. With the modification, accumulations of the early, on time, and late sample sums account for the computed DC offset estimate.

Regarding claim 8, as recited in claim 7, with the modification, accumulation of the early sample sum accounts for the computed DC offset estimate. The early sample sum corresponds to the claimed first set of samples.

Regarding claim 9, Dutkiewicz et al. does not teach receiving a DC offset from an initial calculator. Nevertheless, one of ordinary skill in the art would have recognized that DC tracking stage 23 provides initial DC offset estimate to DC offset removal 22.

Regarding claim 22, claim 22 is rejected on the same ground as for claim 7 because of similar scope.

Regarding claim 23, claim 23 is rejected on the same ground as for claim 8 because of similar scope.

Regarding claim 24, claim 24 is rejected on the same ground as for claim 9 because of similar scope.

4. Claims 10 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Giallorenzi et al. U.S. Patent 5,867,525, Chalmers U.S. Patent 6,141,372. and Dutkiewicz et al. U.S. Patent 5,629,960 as applied to claim 9 above, and further in view of Lindoff et al. U.S. Patent 6,370,205 B1.

Regarding claim 10, Dutkiewicz et al. does not teach calculating a DC offset estimate using a pilot signal as claimed. Lindoff et al. invention is directed to a method for performing DC-offset compensation in a radio receiver. Figure 2 illustrates a DC-offset compensation apparatus 200 including a DC estimation unit 260, a synchronization unit 220. In column 4, lines 15-20, Lindoff et al. teaches the estimate of the DC-offset is performed by using N pilot symbols from the training sequence in the burst. Because N pilot symbols from the training sequence is known, it would have been obvious for one of ordinary skill in the art at the time of invention that Giallorenzi et al. teachings can be modified to use pilot symbols from training sequence as taught by Lindoff et al. to estimate DC-offset. DC offset can be accurately estimated from known pilot sequences.

Regarding claim 25, claim 25 is rejected on the same ground as for claim 10 because of similar scope.

5. Claims 12-18 and 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Giallorenzi et al. U.S. Patent 5,867,525 in view of Dutkiewicz et al. U.S. Patent 5,629,960.

Regarding claim 12, similar to claim 1 rejection, in column 6 line 20 via column 7 line 65, figure 2 of Giallorenzi et al. invention includes on time accumulator 55, early accumulator 59 and late accumulator 61. The accumulators as taught in Giallorenzi et al. invention correspond to the claimed plurality of accumulators.

Giallorenzi et al. does not expressly teach a maximum identifier as set forth in the claim. Nevertheless, Giallorenzi et al. further teaches that a system processor 70 coupled to the accumulators as discussed above uses early, late and on time outputs to compute early-late timing offset estimation; see column 7, lines 50-60, see also figure 3. With a timing offset estimation, one of average skill in the art would have recognized the maximum output of the accumulators as claimed. The timing offset estimation corresponds to the claimed output to be generated according to the identified maximum output.

Giallorenzi et al. invention lacks a DC offset compensator, and therefore, does not show the plurality of accumulators being coupled with the DC offset compensator. Dutkiewicz et al. invention is directed to a method for reducing the effects of transients on the DC offset tracking stage and the symbol timing recovery stage. In column 3 line 25 via column 4 line 25, figure 3 discloses a system including an analog-to-digital (A/D) converter 22, a DC offset removal 22,

a DC tracking stage 23, and a symbol timing recover stage 25. The DC tracking stage tracks the mean DC offset and provides a DC offset voltage 32. Giallorenzi et al. and Dutkiewicz et al. teachings are in the same field of endeavor. As recited in claim 1, DC offset at baseband is often caused by a frequency offset at the receiver relative to the transmitter. As result of that, DC offset estimation is required to eliminate a residual DC signal resulting from the process of down-converting the received signal to baseband. In view of that, it would have been obvious for one of ordinary skill in the art at the time of the invention that Giallorenzi et al. teachings can be modified to implement DC offset removal and DC tracking stage as taught in Dutkiewicz et al. invention. With the modification, on time accumulator 55, early accumulator 59 and late accumulator 61 are being coupled with a DC offset removal 22, which corresponds to the claimed DC offset compensator.

Regarding claim 13, as recited in claim 12, the receiver in figure 2 includes an on time accumulator. Figure 7 illustrates another embodiment in Giallorenzi et al. invention wherein the early/late offset estimator 96 outputs a timing offset estimate for sending to a user for adjusting symbol timing responsive to the early/late offset estimator 96. The early/late offset estimator 96 corresponds to the claimed maximum identifier. The timing offset estimate in figure 7 corresponds to the claimed symbol clock control.

Regarding claim 14, referring to Dutkiewicz et al. invention, as recited in claim 12, in column 3 line 25 via column 4 line 25, figure 3 discloses a system including an analog-to-digital (A/D) converter 22, a DC offset removal 22, a DC tracking stage 23, and a symbol timing recover stage 25. The DC tracking stage 23 tracks the mean DC offset and provides a DC offset voltage 32 to the DC offset removal 22, which corresponds to the claimed DC offset compensator.

Regarding claim 15, Giallorenzi et al. teachings apply to cellular phone technology as stated in the invention.

Regarding claim 16, Giallorenzi et al. does not teach the receiver is a personal digital assistant. However, if a personal digital assistant can be configured to include the receiver as claimed, it would have been for one of ordinary skill in the art at the time of invention that Giallorenzi et al. teachings can be modified to include in a personal digital assistant. The recitation of a new intended use for an old product does not make a claim to that old product patentable. *In re Schreiber, 44 USPQ2d 1429 (Fed. Cir. 1997).*

Regarding claim 17, as recited in claim 15, Giallorenzi et al. teachings apply to cellular phone technology. Because the receiver is part of a cellular device, the receiver can be considered as a peripheral device.

Regarding claim 18, as recited in claim 12, the plurality of accumulators are on time accumulator 55, early accumulator 59 and late accumulator 61.

Regarding claim 26, claim 26 is rejected on the same ground as for claim 12 because of similar scope. Furthermore, the receiver in figure 3 of Dutkiewicz et al. invention shows a A/D converter 21, a DC tracking stage 23 connected to the A/D converter 21.

Regarding claim 27, a DC offset removal 22 is disposed intermediate the A/D converter 21 and the DC tracking stage 23. The DC offset removal 22 inherently performs initial estimation subtraction.

Regarding claim 28, claim 26 is rejected on the same ground as for claim 12 because of similar scope. Furthermore, with the combining teachings of Giallorenzi et al. and Dutkiewicz et al., DC offset removal, taught by Dutkiewicz et al., on time accumulator, early accumulator, late accumulator, and processor 70, taught in Giallorenzi et al., constitutes the claimed multi-hypothesis bit synchronizer.

Allowable Subject Matter

4. Claims 4 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Hsieh et al. U.S. Patent 6,643,336 B1 discloses "DC Offset And Bit Timing System And Method For Use With A Wireless Transceiver".

Kroeger et al. U.S Patent 5,768,323 discloses "Symbol Synchronizer Using Modified Early/Punctual/Late Gate Technique".

Kim et al. U.S Patent 5,724,384 discloses "PN Code Sync Device Using An Adaptive Threshold".

Kroeger et al. U.S Patent 5,566,214 discloses "Automatic Noise Normalization And Reacquisition Control For A QPSK Demodulator Symbol Tracking Loop".

Shoji U.S Patent 5,844,935 discloses "CDMA Receiver".

Umetsu U.S Patent 6,236,648 B1 discloses "CDMA Receiver".

Levin et al. U.S Patent 6,229,839 B1 discloses "Method And Apparatus For Time Tracking".

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Tran whose telephone number is 571-272-3007. The examiner can normally be reached on Monday - Friday from 08:00 AM - 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KCT

Khanh Tran 04/28/2005
Examiner KHANH TRAN